REMARKS

Claims 1-20 are pending in the application. Claims 1, 10, 11 and 20 have been amended.

Claim Rejections under 35 U.S.C. § 102

Claims 1-20 were rejected under 35 U.S.C. § 102(b) as being anticipated by Nizar et al., U.S. Patent No. 5,495,615 (hereinafter "Nizar"). Nizar discloses a multiprocessor programmable interrupt controller (MPIC) system for handling interrupt-related messages (See Abstract). These rejections are traversed, in part, because the cited reference fails to teach or suggest a method and apparatus to establish thread priority in a *single* processor. Both the claims and specification of Nizar disclose "a *multi*processor programmable interrupt controller system." (emphasis added)

Examiner states that all the elements featured in the present claims are disclosed in Nizar. Applicant respectfully submits that the elements, as configured and utilized in Nizar, do not anticipate the present invention as claimed. As to claim 11, Examiner states that Nizar discloses an apparatus for establishing thread priority in a processor comprising a memory to store a value to indicate which one of the threads has a higher priority, referring to element 306 in Fig. 8 and col. 20, ll. 6-9. Applicant submits that Nizar teaches a method and apparatus to prioritize multiple processors within and between multiple clusters of processors, referred to as operating in "intra-cluster" or "inter-cluster" systems (please see col.11, l. 64 to col. 12, l. 60). Applicant's invention relates to use within "a single" processor, which can be found in the specification, and notably, within the preamble of the independent claims. Specifically, Applicant's method and apparatus can be used within the sub-modules of a processor, implemented at each of the stages in an execution pipeline.

Applicant has amended the claims to more clearly define the invention. Claims 1, 10 and 11 and 20 have been rewritten to include the word "single." Applicant's specification and claims support and disclose the method and apparatus utilized in a single *multithreaded* processor system. No new matter has been added.

As per claims 12-19, Examiner's rejections are rendered moot in light of the amended claims. Applicant respectfully submits, that claims 12-19 are allowable as depending from an allowable base claim. Further, Examiner indicates that the other features claimed in 12-19 are disclosed in Nizar. Applicant respectfully submits that, while Nizar discloses the use of a multiprocessor interrupt controller, multithreaded processors are not discussed therein. For example, Examiner refers to the queues in Nizar, for storing bus requests from a plurality of threads, referring to col. 11, ll. 40-43. There, Nizar discusses the use of queues that the "Receive Logic 603 includes a queue for temporarily storing destination address information designating the intended target clusters and logic for decoding the target address." However, Applicant teaches that multiple queues can be used at each stage of the execution pipeline in a multithreaded processor (please see elements 13, 23, 29, 27 and 43 in Fig. 2). These queues can be used to store instructions from various threads and permit higher priority threads to have greater access to the pipeline execution units, as claimed by Applicant. As such, Nizar does not anticipate the apparatus and method of establishing thread priority in a processor; notably, in various stages of the execution pipeline in coordination with the sub-modules within the multithreaded processor system.

Claims 20 and 10 have been rewritten to more clearly define the invention. Applicant submits, therefore that claims 20 and 10 are allowable for the arguments as set forth above. As per claims 1-10, the method claims were rejected upon the same basis as the apparatus structure

of claims 11-20. As previously noted, claim 1 has been rewritten and resembles the independent apparatus structure of claim 11. Hence, the foregoing arguments addressing Examiner's rejections should be applied to claims 1-10.

Based on the amendments and arguments above, reconsideration and withdrawal of the rejection of claims 1-20 under 35 U.S.C. § 102(b) is respectfully requested.

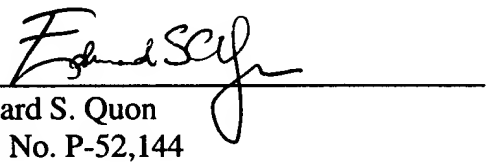
CONCLUSION

For all the above reasons, the Applicant respectfully submits that this application is in condition for allowance. A Notice of Allowance is earnestly solicited.

The Examiner is invited to contact the undersigned at (408) 975-7500 to discuss any matter concerning this application. The Office is hereby authorized to charge any additional fees or credit any overpayments under 37 C.F.R. § 1.16 or § 1.17 to Deposit Account No. 11-0600.

Respectfully submitted,
KENYON & KENYON

Dated: July 08 2002

By: 

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Version with markings to show changes made ("Marked-Up" Version):

Claims (Marked-Up):

A "**marked-up**" version of each claim follows:

1. (Amended) A method of establishing thread priority in a single processor comprising:

assigning a value in memory to indicate which of a plurality of threads executed by said single processor has a higher priority.

10. (Amended) A method of establishing thread priority in a single processor comprising:

assigning a value in an APIC TPR register for a thread via execution of operating system code to indicate which of a plurality of threads executed by said single processor has a higher priority.

11. (Amended) An apparatus for establishing thread priority in a single processor comprising:

a memory to store a value to indicate which of a plurality of threads to be executed by said single processor has a higher priority.

20. (Amended) An apparatus for establishing thread priority in a single processor comprising:

an APIC TPR register for a thread wherein execution of operating system code causes a value to be stored in said register to indicate which of a plurality of threads to be executed by said single processor has a higher priority.